CSC Conflict Resolution

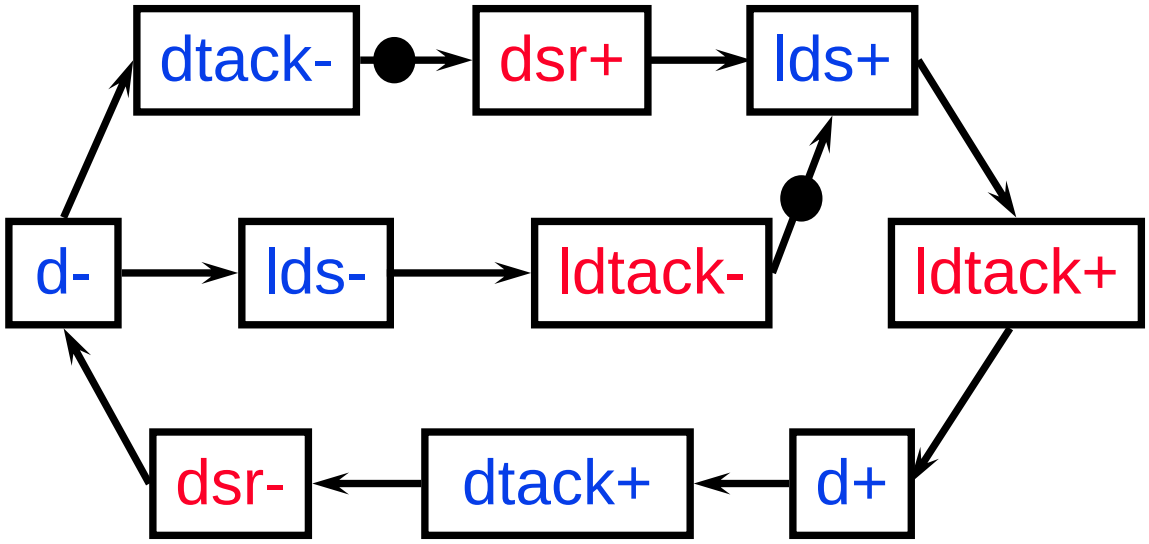
Victor.Khomenko@ncl.ac.uk

School of Computing,

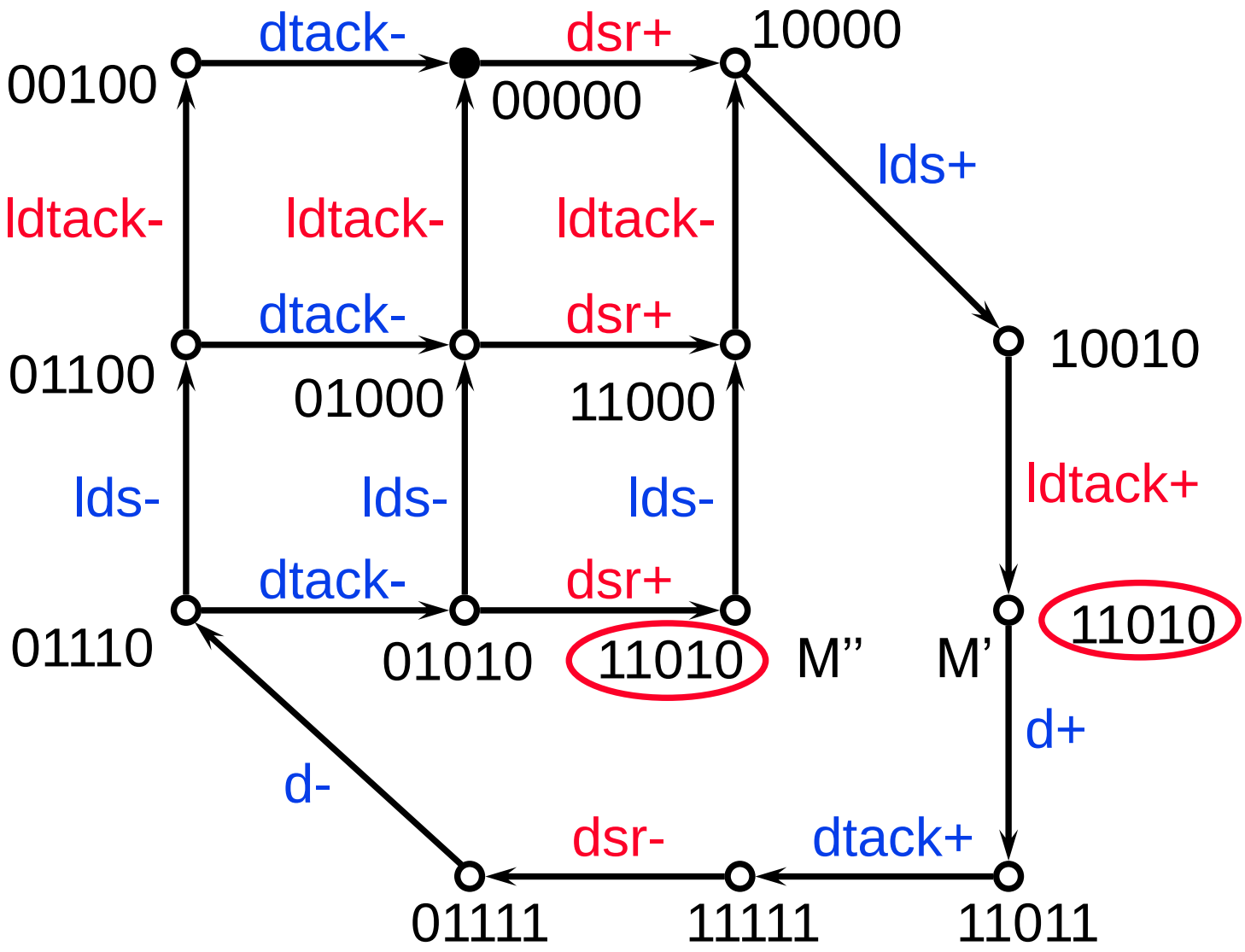
Newcastle University, UK

Online tutorial available from workcraft.org

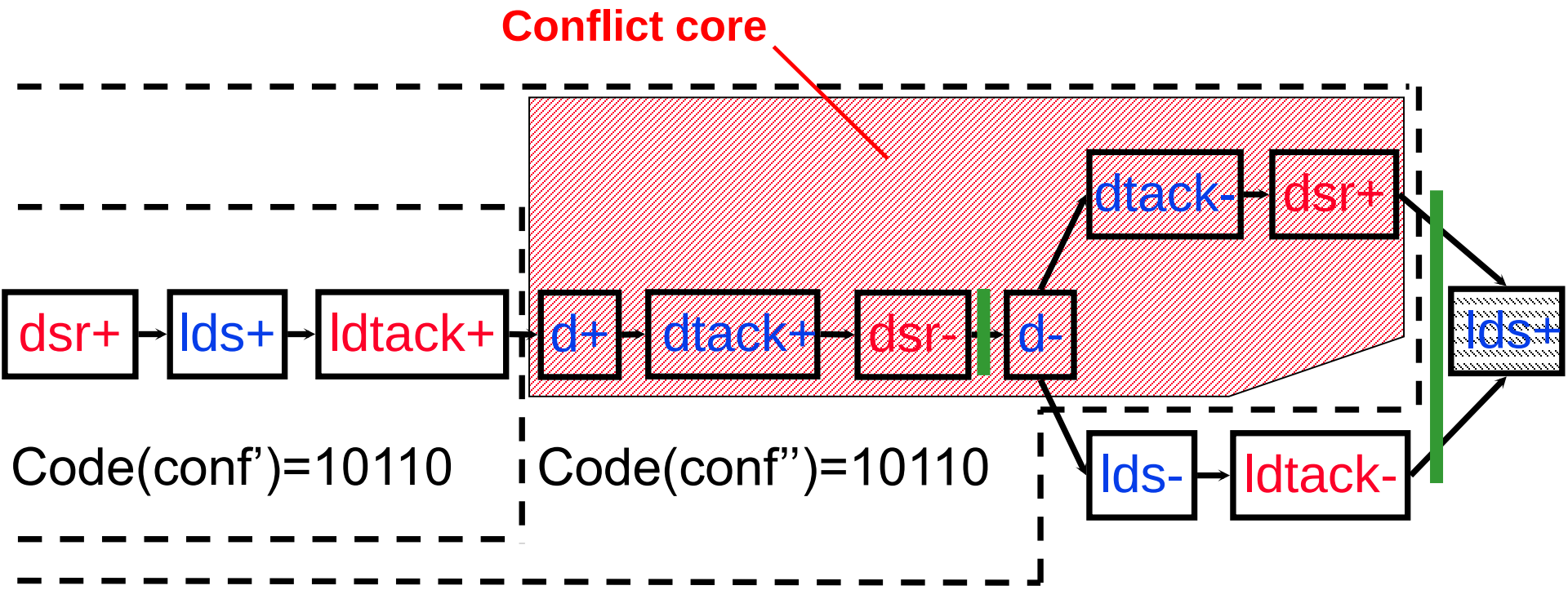
Example: VME Bus Controller



Example: CSC conflict



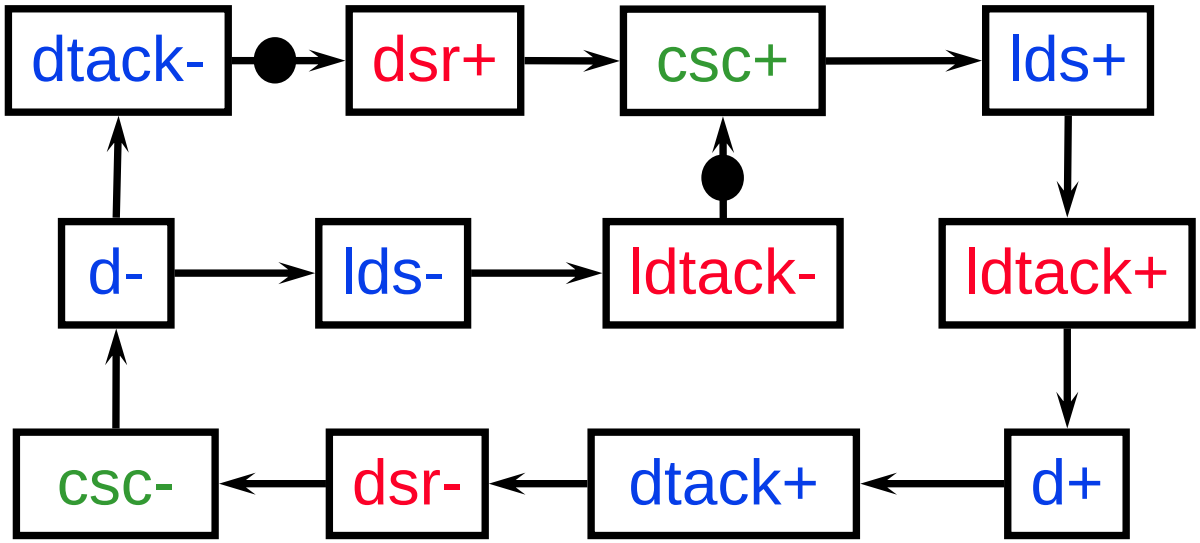
Example: Resolving the conflict



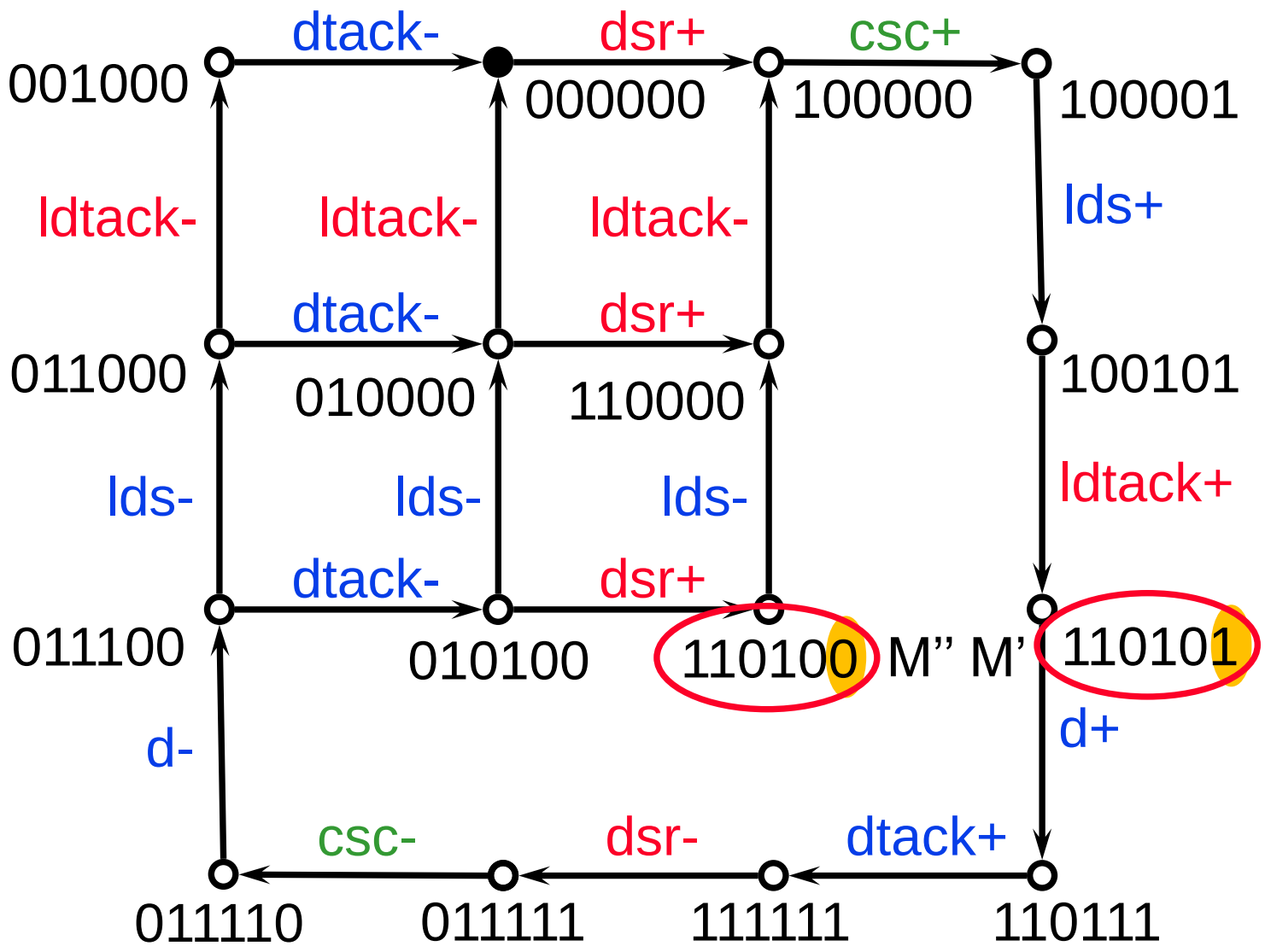
Idea: Insert csc+ into the core and csc- outside the core to break the balance

Note: Cannot delay inputs!

Example: Resolving the conflict

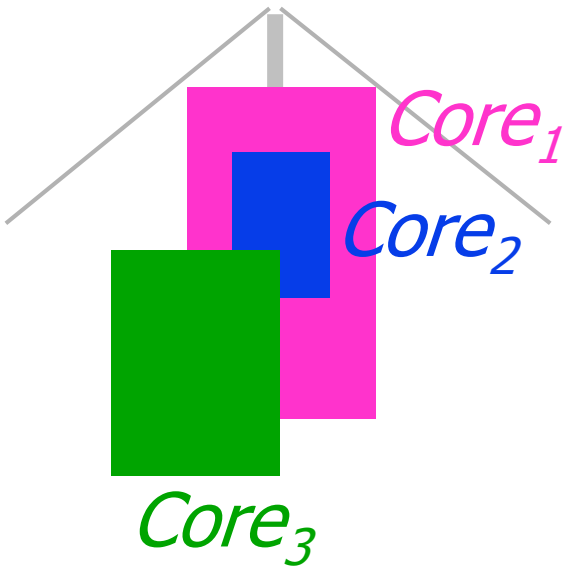


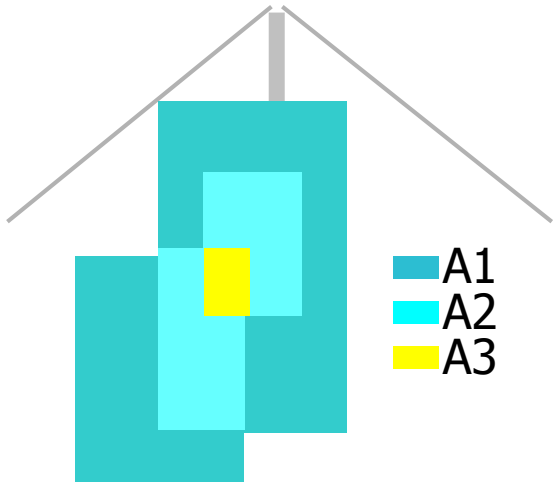
Example: Resolving the conflict

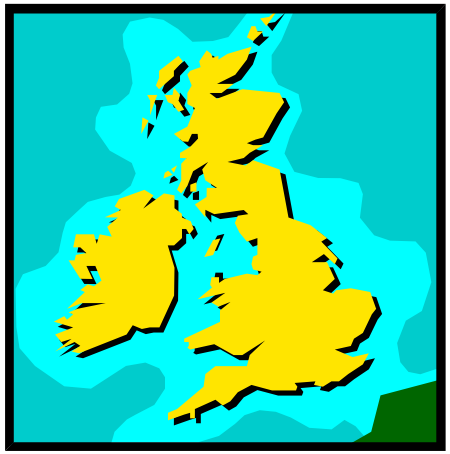


Core map

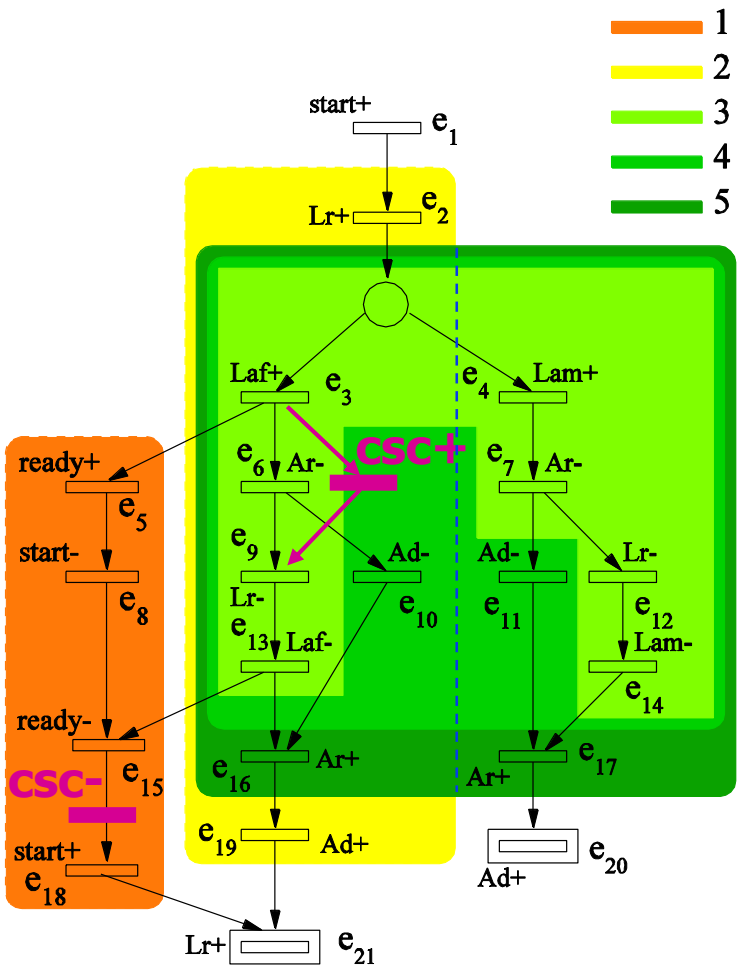
- Cores often overlap
- High-density areas are good candidates for signal insertion
- Analogy with topographic maps







Example: core map



Concurrency reduction

Introduces a new arc in the STG: a → b

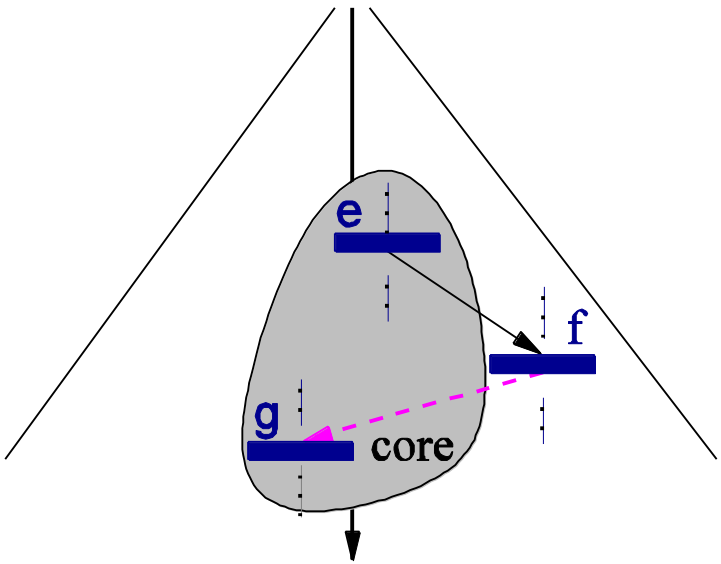
Note: Must not delay inputs, i.e. b cannot be an input!

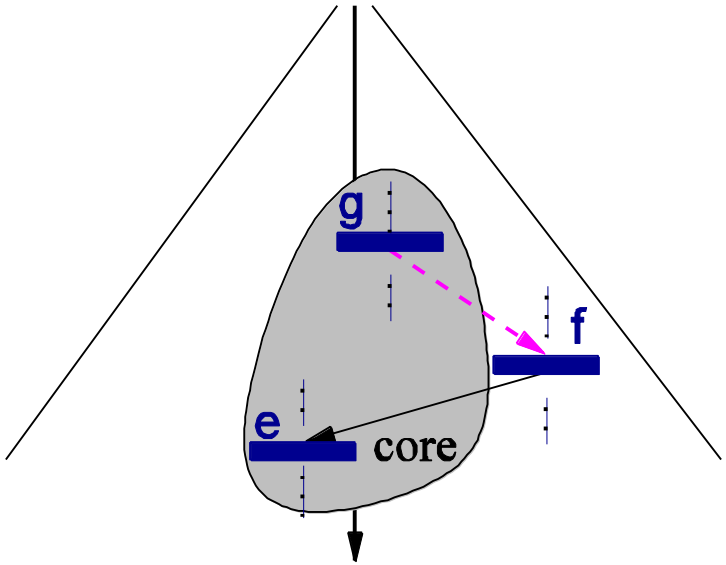
Note: Changes the behaviour, impacts the environment!

Heuristic: Try not to introduce new triggers of b, e.g. if there is an arc a+ → b+ then a- → b- is preferred

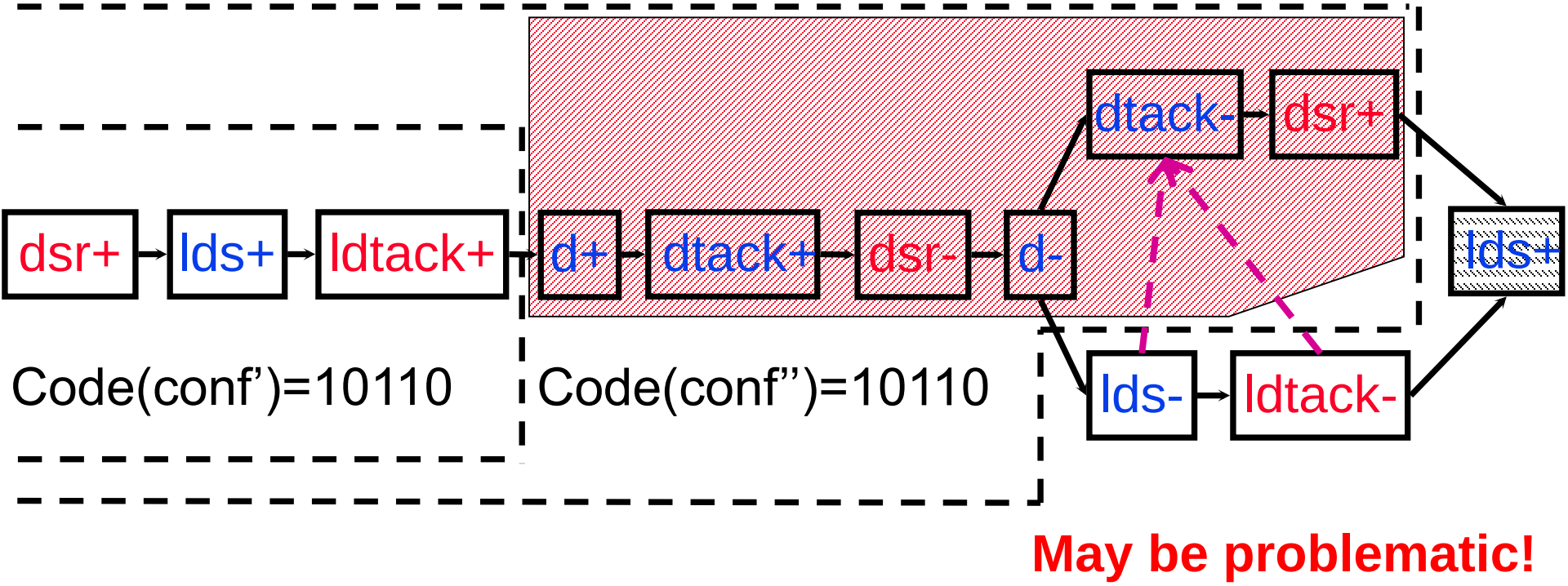
Used for resolving CSC conflicts and circuit simplification

'Drag' some events into the core to break the balance:



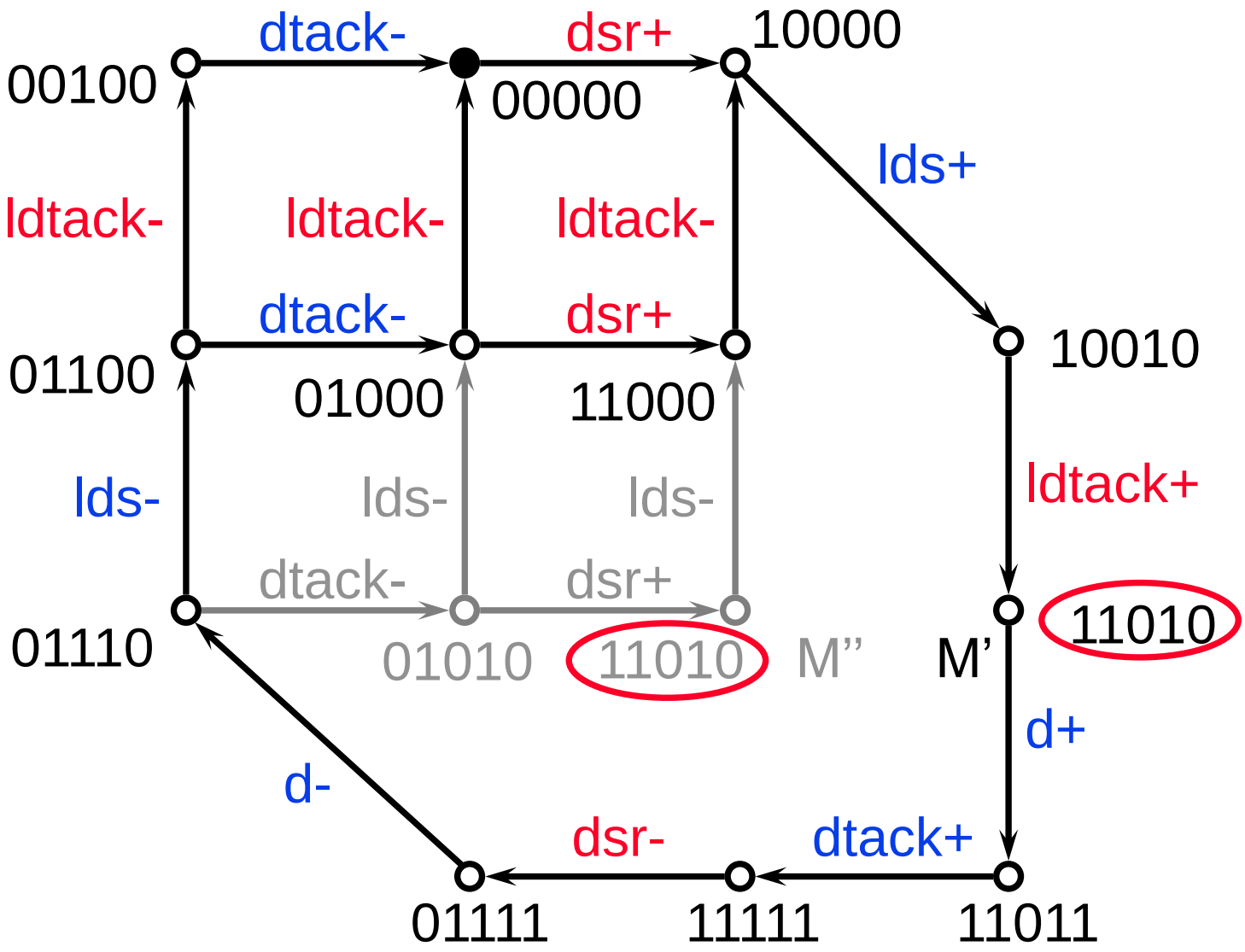


Example: Resolving the conflict



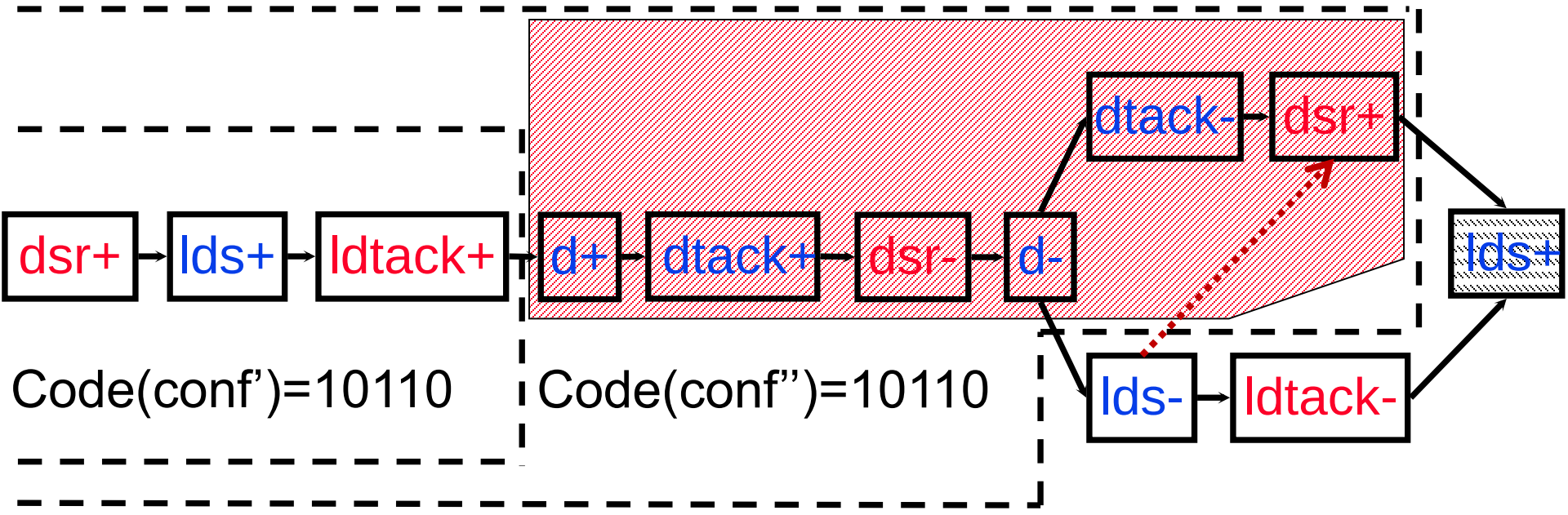
May be problematic!

Example: Resolving the conflict

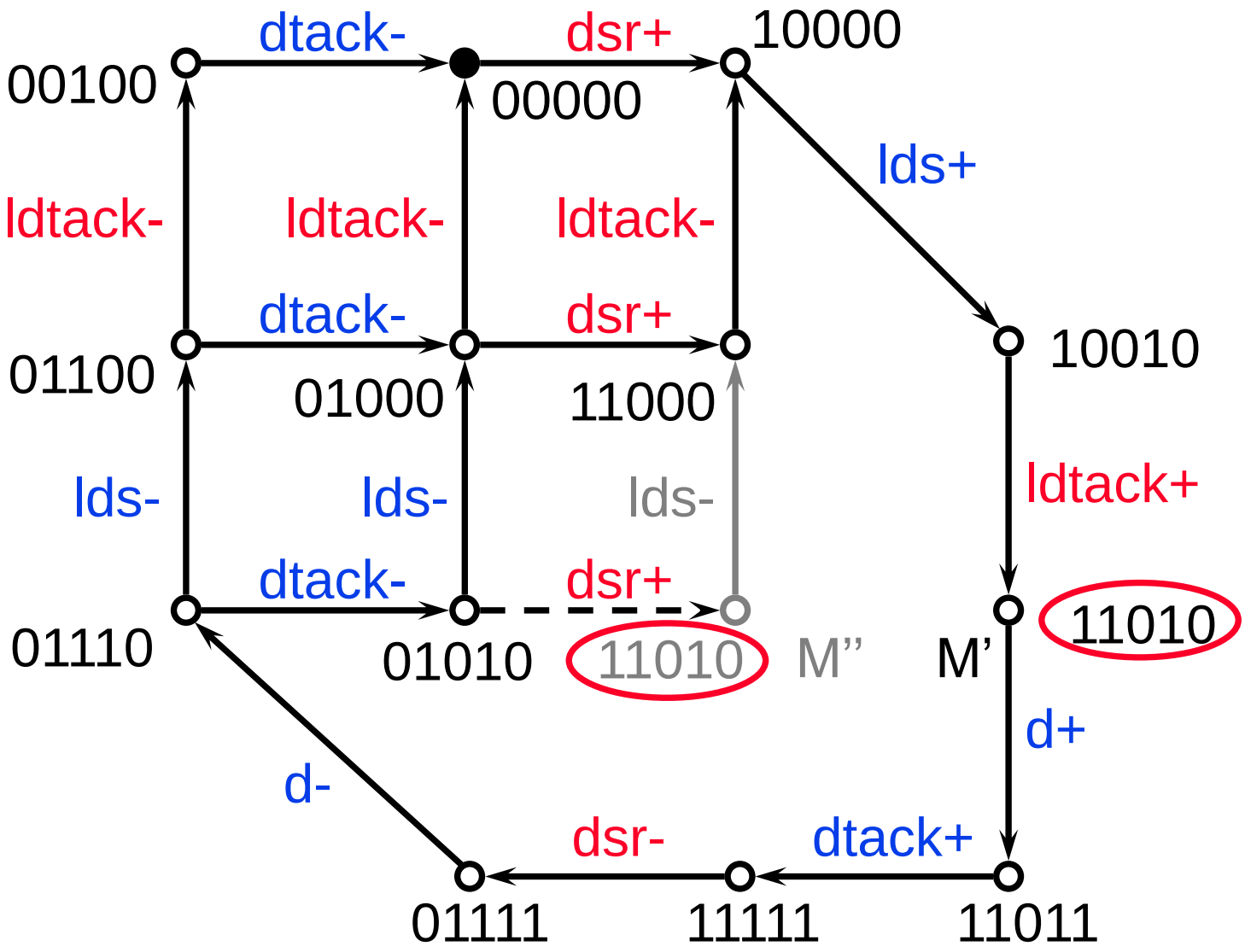


Relative timing assumptions

- "This event will happen faster than that one"
- Break speed-independence, require care & tool support
- Similar to concurrency reductions, but the introduced arcs are special, in particular they don't trigger signals
- Can "delay" inputs



Example: Resolving the conflict



Comparison of the methods

- **Signal insertions – paracetamol**
  - ☺ behaviour is preserved
  - ☹ inserted signals have to be implemented
- **Concurrency reductions – antibiotic**
  - ☺ no new signals
  - ☺ reduced state graph and so more don't-cares in minimisation tables
  - ☹ change the behaviour: need to be careful if input → output (even indirectly) – this puts a new assumption on the environment!
  - ☹ can introduce deadlocks: Circuit: a → b & Environment: b → a
- **Timing assumptions – surgery**
  - ☺ no new signals
  - ☺ reduced state graph and so more don't-cares in minimisation tables
  - ☹ break speed-independence
  - ☹ require deep understanding of theory and the circuit's behaviour
  - ☹ introduce layout constraints, and need care & tool support
  - ☹ fragile due to variability (manufacturing, temperature, voltage, etc.)

Online tutorial:
workcraft.org